APPENDIX A
"Clean" Version of Each Paragraph/Section/Claim
37 CFR 1.121(b)(ii) AND (c)(i)

SPECIFICATION:

Paragraph at page 1, lines 2-3:

B1 This is a division of application Serial No. 09/031,981, filed February 26, 1998, now U.S. Patent No. 6,445,255.

Paragraph at page 2, lines 4-18:

Meanwhile, since the distribution of electromagnetic field around input/output sections of electronic components, such as semiconductor devices, and the distribution of electromagnetic field around planar dielectric lines generally differ, merely mounting electronic component onto the planar dielectric line causes the conversion loss to increase greatly. Further, if electronic components are only mounted onto one surface of the dielectric plate, no connection is made between the electro magnetic field on the back surface thereof and the electronic components, this point also leading to an increase in the conversion loss. Mounting electronic components onto both surfaces of the dielectric plate eliminates the latter problem; however, this results in a decrease in the yield, an increase in loss, and an increase in the material and mounting costs.

B2

Paragraph at page 13, line 6 to page 14, line 9:

Fig. 5 is a view showing the conductor patterns of the main portion of the top surface of the circuit substrate 30. In Fig. 5, reference numerals 12 and 13 each denote a slot line, which is formed in each of the end portions of two planar dielectric line. Reference numerals 10 and 11 each denote a line-conversion conductor pattern, which is formed in the shape of a dipole antenna, as indicated by 10a, 10b, 11a, and 11b,

B3

respectively. Other shapes of the portions 10a, 10b, 11a and 11b are possible as long as the portions function as dipole antennas. The base portions of the line-conversion conductor patterns 10 and 11 form impedance matching sections R which are tapered moderately from the slot lines 12 and 13 toward the line-conversion conductor patterns 10 and 11 in order that the wiring resistance of the line-conversion conductor patterns 10 and 11 is reduced to decrease the conversion loss. If the wavelength of the frequency in the used frequency band in each of the electrode patterns 10a, 10b, 11a and 11b and the impedance matching section R is denoted as λ, they have a length of nearly $\lambda/4$, and the width of the slot lines 12 and 13 is determined by the characteristics impedance of the designed line. Assuming that Z_1 is the input impedance of a portion 100, Z_{01} is the impedance of a portion L_1 and Z_{02} is the impedance of a portion L_2, it is preferable that the relation of these values is given by the following equation:

B3 Cont.

Paragraph at page 19, line 1 to page 20, line 7:

Fig. 7 is a perspective view in a state in which the circuit substrate 30 is placed on the lower conductor plate 44. This VCO is such that a resonator and a variable capacitive element are provided in the high-frequency amplifier shown in Fig. 1B. In Fig. 7, reference numeral 61 denotes a thin-film resistor, with the termination portion of the slot 14 formed on the top surface of the circuit substrate 30 being formed into a tapered shape and this thin-film resistor 61 being provided thereon. Reference numeral 74 denotes another slot provided on the top surface of the circuit substrate 30 and, as will be described later, a slot is also provided on the back-surface side of the circuit substrate 30 with the circuit substrate 30 interposed in between, forming the planar dielectric line. Reference numeral 60 denotes a variable capacitive element mounted in such a manner as to be extended over a slot 74, whose capacitance varies according to an applied voltage. As this variable capacitive element, a variable capacitive capacitor disclosed in Japanese Unexamined Patent Publication No. 5-74655, and a conventional variable capacitive diode may be used. Reference numeral 64 in the figure denotes a section where no conductor is

B4